Advantech

AQD-SD4U16GN32-SE
Datasheet

Rev. 0.0

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Description

AQD-SD4U16GN32-SE is a DDR4 3200Mbps SO-DIMM high-speed, memory module that use 16pcs of 1024M x 8 bits DDR4 SDRAM in FBGA package and a 4K bits serial EEPROM on a 260-pin printed circuit board.

AQD-SD4U16GN32-SE is a Dual In-Line Memory Module and is intended for mounting into 260-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

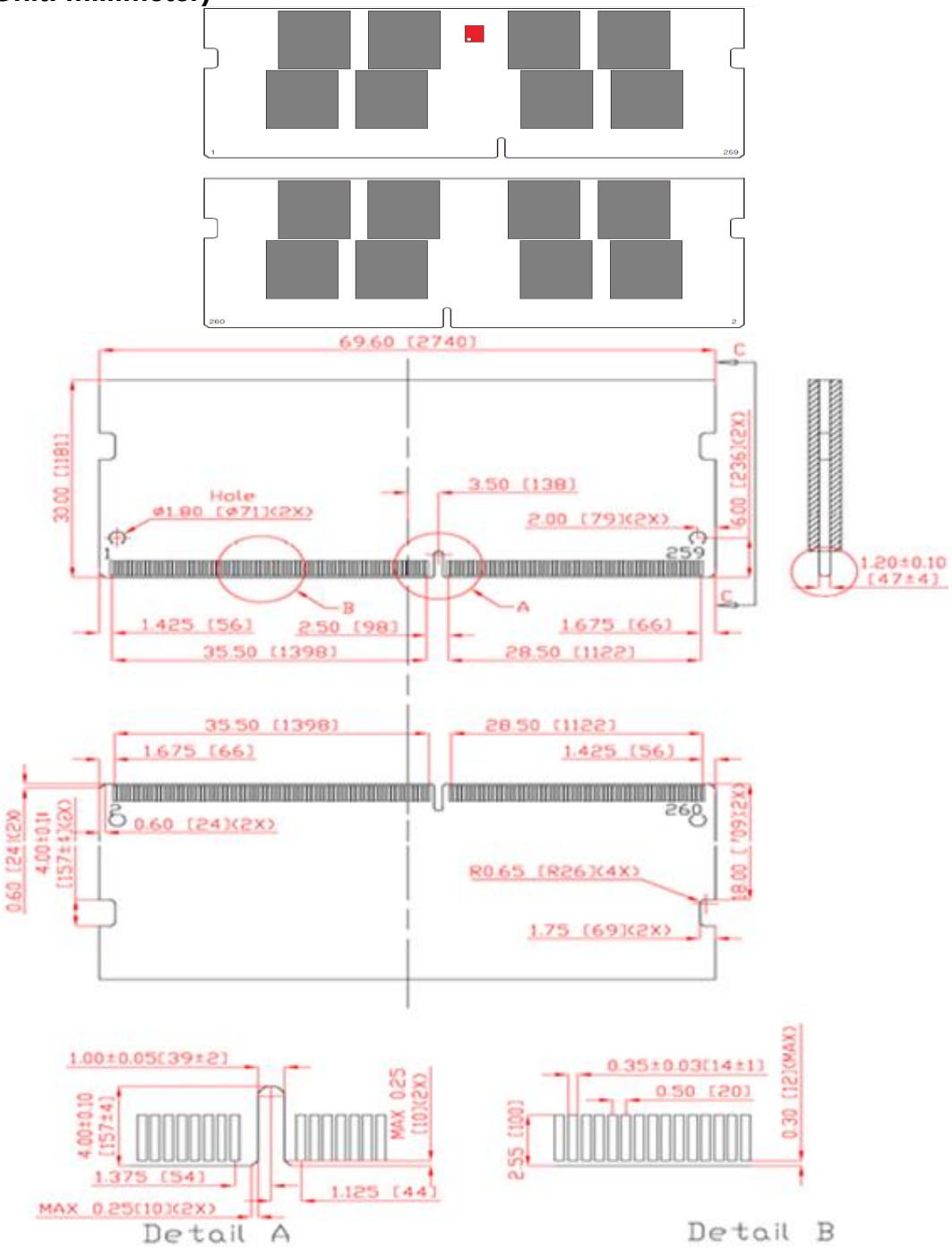
- RoHS compliant products.
- JEDEC standard 1.2V(1.14V~1.26V) Power supply
  VDDQ= 1.2V(1.14V~1.26V)
- VPP = 2.5V +0.25V / -0.125V
- Data transfer rates: PC4-3200
  Programmable CAS Latency: 11~22
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park, and Dynamic ODT
- Serial presence detect with EEPROM
  Asynchronous reset
  PCB edge connector treated with 30u" Gold-Plating
- Anti - sulfur resistor used

Pin Identification

Symbol	Function
A0–A17[1], BA0~BA1	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0_t–DQS17_t	Data Buffer data strobes
DQS0_c–DQS17_c	Data Buffer data strobes
CK0_t, CK1_t	Register clock input
CK0_c, CK1_c	Registert clocks input
ODT0 &ODT1	On-die termination control line
CS0_n–CS3_n	DIMM Rank Select Lines input.
RAS_n[2]	Row address strobe
CAS_n[3]	Column address strobe
WE_n[4]	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
$V_{REF}CA$	Command/address reference supply
$V_{DD}SPD$	SPD EEPROM power supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
RESET_n	Set DRAMs Known State
VTT	DRAM I/O termination supply
VPP	SDRAM Supply
ALERT_n	Register ALERT_n output
EVENT_n	SPD signals a thermal event has occurred
RFU	Reserved for future use

1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Dimensions (Unit: millimeter)

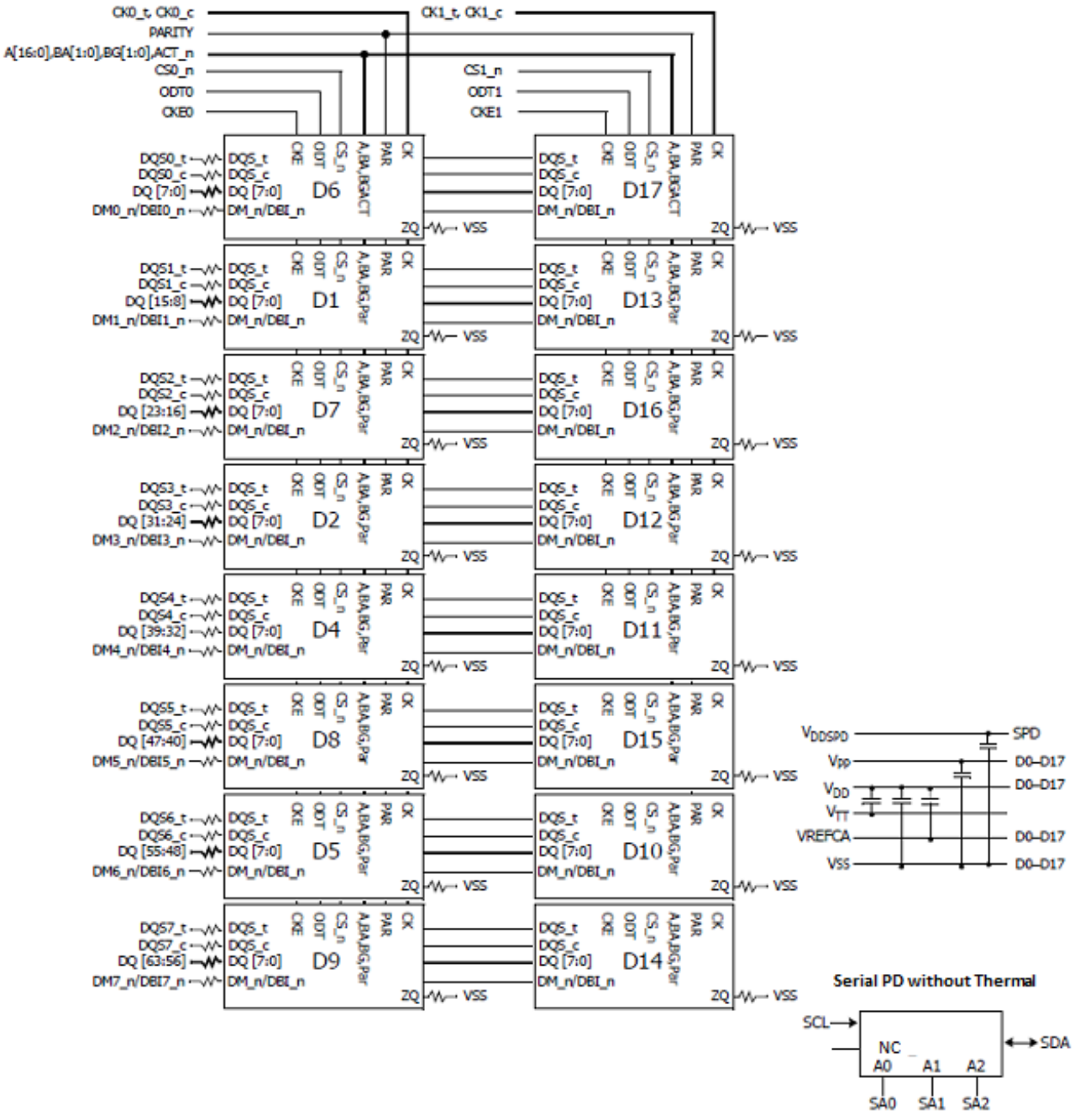


Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	12V	41	DQ10	81	VSS	121	A9	161	ODT1	201	VSS	241	D M7_n/D BI7_n
2	VSS	42	DQ11	82	VSS	122	A7	162	C0,CS2_n,NC	202	VSS	242	DQS7_t
3	DQ5	43	VSS	83	DQ26	123	VSS	163	VDD	203	DQ46	243	VSS
4	DQ4	44	VSS	84	DQ27	124	DQ54	164	VREFCA	204	DQ47	244	VSS
5	VSS	45	DQ21	85	VSS	125	VSS	165	C1,CS3_n,NC	205	VSS	245	DQ62
6	VSS	46	DQ20	86	VSS	126	DQ50	166	SA2	206	VSS	246	DQ63
7	DQ1	47	VSS	87	CB5, NC	127	VSS	167	VSS	207	DQ42	247	VSS
8	DQ0	48	VSS	88	CB4, NC	128	DQ60	168	VSS	208	DQ43	248	VSS
9	VSS	49	DQ17	89	VSS	129	VDD	169	DQ37	209	VSS	249	DQ58
10	VSS	50	DQ16	90	VSS	130	VDD	170	DQ36	210	VSS	250	DQ59
11	DQ S0_c	51	VSS	91	CB1, NC	131	A3	171	VSS	211	DQ52	251	VSS
12	D M0_n/D BI0_n, NC	52	VSS	92	CB0, NC	132	A2	172	VSS	212	DQ53	252	VSS
13	DQS0_t	53	DQ S2_c	93	VSS	133	A1	173	DQ33	213	VSS	253	SCL
14	VSS	54	D M2_n/D BI2_n, NC	94	VSS	134	EVENT_n	174	DQ32	214	VSS	254	SDA
15	VSS	55	DQS2_t	95	DQ S8_c	135	VDD	175	VSS	215	DQ49	255	VDDSPD
16	DQ6	56	VSS	96	D M8_n/D BI8_n, NC	136	VDD	176	VSS	216	DQ48	256	SA0
17	DQ7	57	VSS	97	DQ S8_t	137	CK0_t	177	DQS4_c	217	VSS	257	VPP
18	VSS	58	DQ22	98	VSS	138	CK1_t	178	D M4_n/D BI4_n	218	VSS	258	VTT
19	VSS	59	DQ23	99	VSS	139	CK0_c	179	DQS4_t	219	DQS6_c	259	VPP
20	DQ2	60	VSS	100	CB6, NC	140	CK1_c	180	VSS	220	D M6_n/D BI6_n, NC	260	SA1
21	DQ3	61	VSS	101	CB2, NC	141	VDD	181	VSS	221	DQS6_t		
22	VSS	62	DQ18	102	VSS	142	VDD	182	DQ39	222	VSS		
23	VSS	63	DQ19	103	VSS	143	PARITY	183	DQ38	223	VSS		
24	DQ12	64	VSS	104	CB7, NC	144	A0	184	VSS	224	DQ54		
25	DQ13	65	VSS	105	CB3, NC	145	BA1	185	VSS	225	DQ55		
26	VSS	66	DQ28	106	VSS	146	A10/AP	186	DQ35	226	VSS		
27	VSS	67	DQ29	107	VSS	147	VDD	187	DQ34	227	VSS		
28	DQ8	68	VSS	108	RESET_n	148	VDD	188	VSS	228	DQ50		
29	DQ9	69	VSS	109	CKE0	149	CS0_n	189	VSS	229	DQ51		
30	VSS	70	DQ24	110	CKE1	150	BA0	190	DQ45	230	VSS		
31	VSS	71	DQ25	111	VDD	151	A14/WE_n	191	DQ44	231	VSS		
32	DQ S1_c	72	VSS	112	VDD	152	A16/RAS_n	192	VSS	232	DQ60		
33	D M1_n/D BI1_n, NC	73	VSS	113	BG1	153	VDD	193	VSS	233	DQ61		
34	DQS1_t	74	DQ S3_c	114	ACT_n	154	VDD	194	DQ41	234	VSS		
35	VSS	75	D M3_n/D BI3_n, NC	115	BG0	155	ODT0	195	DQ40	235	VSS		
36	VSS	76	DQ S3_t	116	ALERT_n	156	A15/CAS_n	196	VSS	236	DQ57		
37	DQ15	77	VSS	117	VDD	157	CS1_n	197	VSS	237	DQ56		
38	DQ14	78	VSS	118	VDD	158	A13	198	DQS5_c	238	VSS		
39	VSS	79	DQ30	119	A12	159	VDD	199	D M5_n/D BI5_n	239	VSS		
40	VSS	80	DQ31	120	A11	160	VDD	200	VSS	240	DQS7_c		

16GB, 1Gx8 Module (2 Rank x8)



Note:

1. Unless otherwize noted, resistor values are 15Ω±5%.
2. ZQ resistors are 240Ω±1%.For all other resistor values refer to the appropriate wiring diagram.

- This technical information is based on industry standard data and tests believed to be reliable. However, Advantech makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Advantech reserves the right to make changes in specifications at any time without prior notice.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.3 ~ 1.5	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Supply voltage	VDD	1.2V	1.14	1.2	1.26	V	1,2,3
Supply voltage for Output	VDDQ	1.2V	1.14	1.2	1.26	V	1,2,3
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	1.2V	0.49*VDD	0.50*VDD	0.51*VDD	V	4
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	1.2V	0.49*VDD	0.50*VDD	0.51*VDD	V	4
AC Input Logic High	VIH(AC)	1.2V	VREF+90	-	VDD^2	mV	
AC Input Logic Low	VIL(AC)	1.2V	VSS^2	-	VREF–90	mV	
DC Input Logic High	VIH(DC)	1.2V	VREF+65	-	VDD	mV	
DC Input Logic Low	VIL(DC)	1.2V	VSS	-	VREF-65	mV	

Note:
(1) Under all conditions VDDQ must be less than or equal to VDD.
(2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
(3) The DC bandwidth is limited to 20MHz.
(4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

IDD Specification parameters Definition - 16GB (2 Rank x8)

Parameter	Symbol	DDR4 3200 CL22	Unit
One bank ACTIVATE-PRECHARGE current	IDD0[1]	352	mA
One bank ACTIVATE-PRECHARGE, wordline boost, IPP current	IPP0[1]	64	mA
One Bank Active-Read-Precharge Current	IDD1[1]	376	mA
Precharge Standby Current	IDD2N[2]	320	mA
Precharge standby ODT current	IDD2NT[1]	280	mA
Precharge Power-Down Current	IDD2P[2]	208	mA
Precharge Quiet Standby Current	IDD2Q[2]	320	mA
Active standby current	IDD3N[2]	480	mA
Active standby IPP current	IPP3N[2]	64	mA
Active Power-Down Current	IDD3P[2]	336	mA
Burst Read Current	IDD4R[1]	1016	mA
Burst write current	IDD4W[1]	952	mA
Burst refresh current (1x REF)	IDD5B[1]	1944	mA
Burst refresh IPP current (1x REF)	IPP5B[1]	232	mA
Self refresh current: Normal temperature range (0–85°C)	IDD6N[2]	336	mA
Self refresh current: Extended temperature range (0–95°C)	IDD6E[2]	512	mA
Bank interleave read current	IDD7[1]	1368	mA
Bank interleave read IPP current	IPP7[1]	120	mA
Maximum power-down current	IDD8[2]	176	mA

Note: 1. One module rank in the active IDD/PP, the other rank in IDD2P/PP3N.
2. All ranks in this IDD/PP condition.
3.IDD current measure method and detail patterns are described on DDR4 component datasheet. Only for reference.

■ Timing Parameters & Specifications

SERIAL PRESENCE DETECT SPECIFICATION (AQD-SD4U16GN32-SE Serial Presence Detect)

Byte	Function Described	Function		HEX Value
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	SPD Total: 512Bytes, SPD Used : 384Bytes		23
1	SPD Revision	Version 1.1		11
2	Key Byte / DRAM Device Type	DDR4 SDRAM		0C
3	Key Byte / Module Type	SO-DIMM		03
4	SDRAM Density and Banks	4 bank group / 4 bank	8Gb	85
5	SDRAM Addressing	Row : 16	Column : 10	21
6	SDRAM Package Type	Mono / Not specified		00
7	SDRAM Optional Features	Unlimited MAC		08
8	SDRAM Thermal and Refresh Options	-		00
9	Other SDRAM Optional Features	hPPR,sPPR supported		60
10	Reserved	-		00
11	Module Nominal Voltage, VDD	1.2v		03
12	Module Organization	2Rank	x8	09
13	Module Memory Bus Width	Non ECC	64bits	03
14	Module Thermal Sensor	Non Thermal Sensor		00
15~16	Reserved	-		00
17	Timebases	MTB: 125ps	FTB: 1ps	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.625 ns		05
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.6 ns		0D
20	CAS Latencies Supported, First Byte	CL 10,11,12,13,14		F8
21	CAS Latencies Supported, Second Byte	CL 15,16,17,18,19,20,22		BF
22	CAS Latencies Supported, Third Byte	CL24		02
23	CAS Latencies Supported, Fourth Byte	-		00
24	Minimum CAS Latency Time(tAAmin)	13.75 ns		6E
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.75 ns		6E
26	Minimum Row Precharge Delay Time (tRPmin)	13.75 ns		6E
27	Upper Nibbles for tRASmin and tRCmin	-		11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	32 ns		00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	45.75 ns		6E
30	Minimum Refresh Recovery Delay Time (tRFC1min), Least Significant Byte	350 ns		F0
31	Minimum Refresh Recovery Delay Time (tRFC1min), Most Significant Byte			0A
32	Minimum Refresh Recovery Delay Time (tRFC2min), Least Significant Byte	260 ns		20
33	Minimum Refresh Recovery Delay Time (tRFC2min), Most Significant Byte			08
34	Minimum Refresh Recovery Delay Time (tRFC4min), Least Significant Byte	160 ns		00
35	Minimum Refresh Recovery Delay Time (tRFC4min), Most Significant Byte			05
36	Minimum Four Activate Window Time (tFAWmin), Most Significant Nibble	21 ns		00
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte			A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	2.5 ns		14
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	4.9 ns		28
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5 ns		28
41	Upper Nibble for tWRmin	15 ns		00
42	Minimum Write Recovery Time(tWRmin)	15 ns		78
43	Upper Nibbles for tWTRmin	2.5/7.5 ns		00
44	Minimum Write to Read Time(tWTR_Smin) , different bank group	2.5 ns		14
45	Minimum Write to Read Time(tWTR_Lmin) , same bank group	7.5 ns		3C
46~59	Reserved, Base Configuration Section	-		00
60	Connector to SDRAM Bit Mapping	DQ0, DQ1, DQ2, DQ3		0B
61	Connector to SDRAM Bit Mapping	DQ4, DQ5, DQ6, DQ7		2B
62	Connector to SDRAM Bit Mapping	DQ8, DQ9, DQ10, DQ11		0C
63	Connector to SDRAM Bit Mapping	DQ12, DQ13, DQ14, DQ15		2B
64	Connector to SDRAM Bit Mapping	DQ16, DQ17, DQ18, DQ19		2B
65	Connector to SDRAM Bit Mapping	DQ20, DQ21, DQ22, DQ23		0B
66	Connector to SDRAM Bit Mapping	DQ24, DQ25, DQ26, DQ27		16
67	Connector to SDRAM Bit Mapping	DQ28, DQ29, DQ30, DQ31		36
68	Connector to SDRAM Bit Mapping	CB0-3		00
69	Connector to SDRAM Bit Mapping	CB4-7		00
70	Connector to SDRAM Bit Mapping	DQ32, DQ33, DQ34, DQ35		15
71	Connector to SDRAM Bit Mapping	DQ36, DQ37, DQ38, DQ39		2C
72	Connector to SDRAM Bit Mapping	DQ40, DQ41, DQ42, DQ43		0B
73	Connector to SDRAM Bit Mapping	DQ44, DQ45, DQ46, DQ47		35
74	Connector to SDRAM Bit Mapping	DQ48, DQ49, DQ50, DQ51		16
75	Connector to SDRAM Bit Mapping	DQ52, DQ53, DQ54, DQ55		36
76	Connector to SDRAM Bit Mapping	DQ56, DQ57, DQ58, DQ59		16

Byte	Function Described	Function		HEX Value
77	Connector to SDRAM Bit Mapping	DQ60, DQ61, DQ62, DQ63		36
78~116	Reserved, Base Configuration Section	-		00
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	0ns		00
118	Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Lmin), different bank group	-0.1ns		9C
119	Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Smin), same bank group	0ns		00
120	Fine Offset for Minimum Activate to Activate/Refresh Delay Time(tRCmin)	0ns		00
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	0ns		00
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCDmin)	0ns		00
123	Fine Offset for Minimum CAS Latency Time(tAAmin)	0ns		00
124	Fine Offset for SDRAM Maximum Cycle Time(tCKAVGmax)	-0.025ns		E7
125	Fine Offset for SDRAM Minimum Cycle Time(tCKAVGmin)	0ns		00
126	Cyclical Redundancy Code for Base Configuration Section, LSB	CRC-CCITT(LOW)		3A
127	Cyclical Redundancy Code for Base Configuration Section, MSB	CRC-CCITT(HIGH)		56
128	(Unbuffered): Raw Card Extension, Module Nominal Height	Revision 1	30.00 mm	0F
129	(Unbuffered): Module Maximum Thickness	-		11
130	(Unbuffered): Reference Raw Card Used	Raw Card E	Revision 1	24
131	(Unbuffered): Address Mapping from Edge Connector to DRAM	Mirrored		01
132~253	(Unbuffered): Reserved	-		00
254	(Unbuffered): CRC for Module Specific Section, Least Significant Byte	CRC-CCITT(LOW)		55
255	(Unbuffered): CRC for Module Specific Section, Most Significant Byte	CRC-CCITT(HIGH)		23
256~319	Hybrid Memory Architecture Specific Parameters			00
320	Module Manufacturer ID Code, LSB			04
321	Module Manufacturer ID Code, MSB			CB
322	Module ID: Module Manufacturing Location	*Note: 1		-
323	Module ID: Module Manufacturing Date(Year)	*Note: 2		-
324	Module ID: Module Manufacturing Date(Week)	*Note: 3		-
325~328	Module ID : Module Serial Number	*Note: 4		-
329~348	Module Part Number	*Note: 5		-
349	Module Revision Code	-		00
350	SDRAM Manufacturer's JEDEC ID Code, LSB	Samsung		80
351	SDRAM Manufacturer's JEDEC ID Code, MSB			CE
352	DRAM Stepping	*Note: 7		-
353~381	Manufacturer's Specific Data	*Note: 8		-
382	Reserved			00
383	Reserved			00
384~511	End User Programmable	*Note: 9		-

Note : 1. Byte 322 -- Manufacturing location by manufacturing location (00:Taiwan /01:China)
2. Byte 323 -- Module manufacturing date by year (YY).
3. Byte 324 -- Module manufacturing date by week (WW).
4. Bytes 325~328 -- Module Serial Number.
5. Bytes 329~348 -- Manufacturer Part Number by module part number , (Unused digits are coded as ASCII blanks (20h)).
6. Bytes 353~381 -- These bytes are undefined and can be used own purpose. Digits are coded as 00h except the following:
   6-1. Bytes 353~367 -- Manufacturer's Specific Data by working order number.
   6-2. Bytes 368~381 -- Manufacturer's Specific Data by SPD naming number.
7. Bytes 384~511 -- These bytes are undefined and can be used own purpose. Digits are coded as 00h except the following:
   7-1. Bytes 384 -- The byte is coded as ADh.