TUL Embedded

96VG-A6600LX8-6T1

Performance PCIe Graphics

4 x Mini DisplayPort

MPN：1A1-E004039ADP

CONTENTS

1. Specification

Model Name	EP23GL-MP4U
Graphics Engine	AMD Radeon RX 6600
Process Node	7 nm
Engine Clock (max)	Base : up to 1089 MHz Boost : up to 1354 MHz Game : up to 1183 MHz *
Graphics Memory	128-bit, 8 GB, GDDR6
Memory Clock (max)	14.0 Gbps
Bus Interface	PCI Express® 4.0 (x8)
Shader Processing Units	1792 Stream processors
Floating Point Performance	4.85 TFLOPs
DirectX® Capability	DirectX® 12
Shader Model	Shader Model 6.1
OpenGL™	OpenGL™ 4.6
OpenCL™	OpenCL™ 2.2
VULKAN™	VULKAN™ Support
Unified Video Decoder (UVD)	Radeon Media Engine
BIOS Mode	UEFI
Display Interface	4 x Mini DisplayPort
Maximum Resolution	DisplayPort: 3840x2160
Power Consumption	70 W
Operating Temperature	0°C ~ 45°C
Dimension	180 x 69 mm

*Note : Game Clock is the expected GPU clock when running typical gaming applications, set to typical TGP (Total Graphics Power). Actual individual game clock results may vary

2. Functional Overview

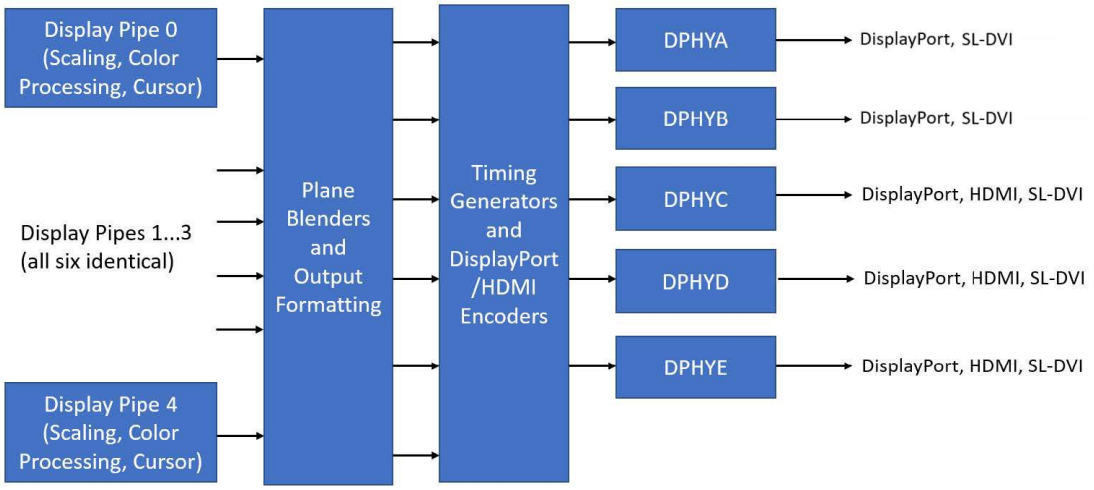
2.1. Memory Interface

AMD Radeon RX 6600 have 8 independent memory channels that provide 128-bit wide memory interface, capable of connecting up to 4 GDDR6 memory chips when configured in ×16 mode.
All the GDDR6 chips connected must be of the same type, and run at the same speed and voltage.

2.2. Acceleration Features

- Support for DirectX® 12 Ultimate:
  - Shader Model 6.1 support in a full-speed 32-bit floating point unified shader architecture
  - Support for Vulkan 1.2.
  - Support for OpenGL 4.6.
  - Support for OpenCL™ 2.2.
  - Anti-aliasing filtering:
    - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
    - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
    - Custom filter anti-aliasing with up to 12-samples per pixel.
    - An adaptive anti-aliasing mode.
    - Lossless color compression (up to 16:1).
  - Anisotropic filtering:
    - Continuous anisotropic with 1× through 16× taps.
    - Up to 128-tap texture filtering with unified non-power of two-tap distribution and higher precision filter computations.
    - Angle-invariant algorithm for improved quality.
    - Anisotropic biasing to allow trading quality for performance.
    - Advanced texture compression (3Dc+™).
    - High quality 4:1 compression for normal and luminance maps.
    - Single- or two-channel data format compatibility.
  - Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
  - Hierarchical z- and stencil-buffers with early z-test.
  - Lossless z-buffer compression for both z and stencil.
  - Fast z-buffer and color-buffer clear.

2.3. Display System



Note: Do not design with HDMI™ connector on Port A or B.

Note: HDMI support is available only to HDMI adopters.

Independent per output content protection support:

- HDMI: HDCP versions 1.4 or 2.3
- DVI: HDCP 1.4
- DP: HDCP 1.1 or 2.3

Note: HDCP is available only to HDCP licensees and can only be enabled when connected to an HDCP-capable receiver.

There is also support for overlays to read independent memory surfaces, independently scale and color process, and alpha blend full screen or in a window on the primary display surface for each display. Each display output stream consumes pipe resources and removes pipes from the pool available for overlays.

Support for Radeon FreeSync™ and FreeSync™ 2 technologies exist on DisplayPort, and HDMI interfaces.

2.4. DisplayPort (DP) Features

- DisplayPort (DP) 1.4a on all ports.
- All lane count options supported: 1, 2, and 4 lanes.
- All link rates up to HBR3 (8.1 Gbps) are supported:
  - Speeds up to HBR2 (5.4 Gbps) enabled at low power level
  - HBR3 (8.1 Gbps) requires increased voltage supply and power

- FEC on all ports.
- Multi-Streaming Transport (MST) allowing up to four video streams per DP port.
- RGB 4:4:4 with 24, 30, or 36 bpp.
- YCbCr 4:4:4, 4:2:2, or 4:2:0 using 8, 10, or 12 bpc.

2.5. HDMI and DVI Features

Supports the following HDMI and Single-Link DVI features on Ports C, D and E.

The Single-Link DVI features can also be supported on Port B.

HDMI TMDS transport up to 6.0 Gbps.

HDMI FRL transport on one output port with DSC (compressed) or uncompressed video transport up to 12G at the low power level. HDMI FRL transport at 6 Gbps (6G) is supported on systems that support 6G TMDS.

The following video timing features of HDMI are supported when FRL is enabled at 6G or higher:

- 4K100A
- 4K100B
- 4K120A
- 4K120B
- 8K50B
- 8K60B

Other select HDMI 2.1 features are supported on all ports using either TMDS or FRL transport subject to driver updates and operating system support:

- Dynamic HDR Metadata transport
- VRR (Variable Refresh Rate) supporting Radeon FreeSync™
- ALLM (Automatic Low Latency Mode)

Single-link DVI 1.0 using 24 bpp RGB up to 165 MPix/sec on all ports at the low power level.

Note: Dual-Link DVI is not supported.

The following features apply to HDMI and not DVI:

- RGB 4:4:4 with 24, 30, or 36 bpp
- YCbCr 4:4:4, 4:2:2, or 4:2:0 using 8, 10, or 12 bpc
- 4:2:0 modes limited to 4K50 and above as per HDMI specification.
- Static HDR support for Rec.2100 PQ (HDR10) and HLG.

2.6. Integrated HD-Audio Controller (Azalia) and Codec

Each HDMI, DisplayPort output supports HD audio stream independently, up to a maximum of five output streams

- The maximum total output bandwidth of all audio streams is 73.728 Mbps.
- The maximum compressed audio bandwidth per stream is 24.576 Mbps.
- The maximum uncompressed audio bandwidth per stream is 36.864 Mbps.

Note: The integrated audio controller is compatible with the Microsoft® UAA driver for basic audio functionality. For advanced functionality, an AMD or a third party driver is required.

Each audio stream can support:

- Uncompressed L-PCM:
  - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
  - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
  - Bits per sample: 16, 20, and 24
- Non-HBR compressed audio pass-through up to 6.144 Mbps:
  - Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD
- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD
- Plug-and-Play:
  - Sink audio format capabilities declaration.
  - Sink information.
  - AV association.
  - Lip sync information.
- HDCP content protection

2.7. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 4.0, up to 16.0 GT/s.
- Supports ×1, ×2, ×4, ×8 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s, and 16.0 GT/s link-data rates.
- Supports ×8 lane reversal where the receivers on lanes 0 to 7 on the upstream port of the chip are mapped to the transmitters on lanes 7 down to 0 on the root port of the root complex.
- Supports ×8 lane reversal where the transmitters on lanes 0 to 7 on the upstream port of the chip are mapped to the receivers on lanes 7 down to 0 on the root port of the root complex (requires corresponding support on the root complex).

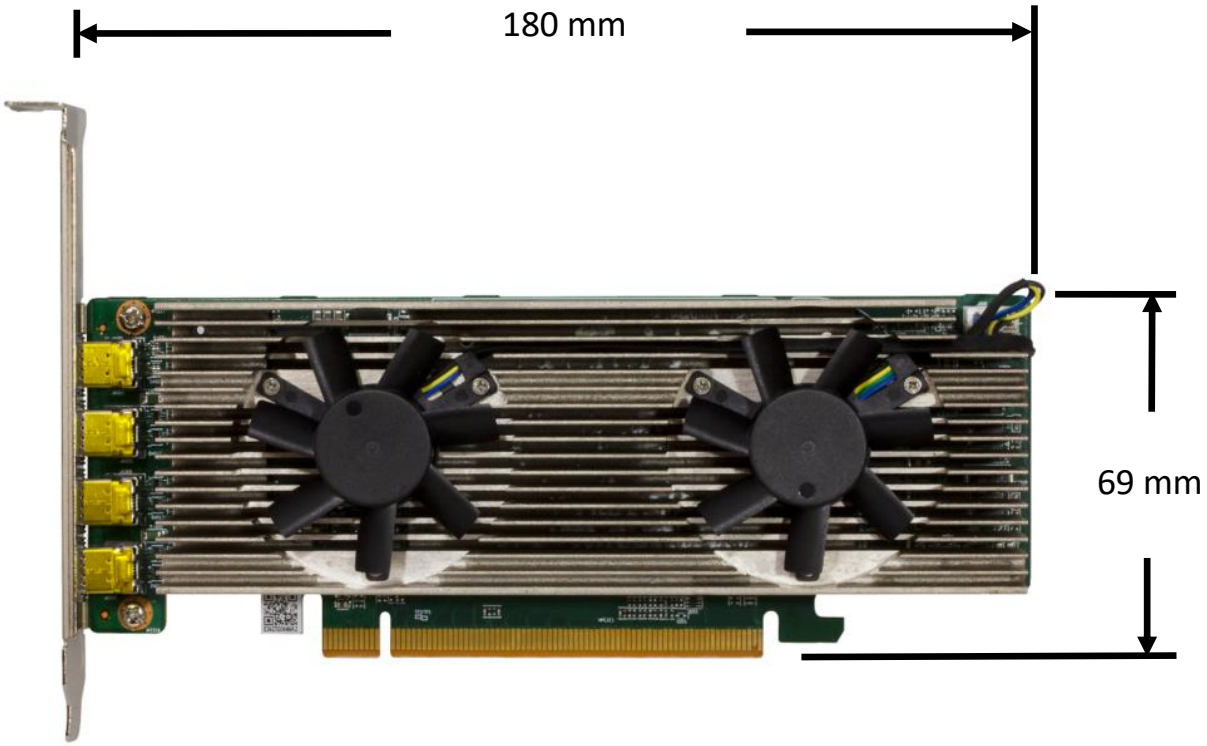
3. PIN Assignment and Description

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair
22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2,	GND	Ground

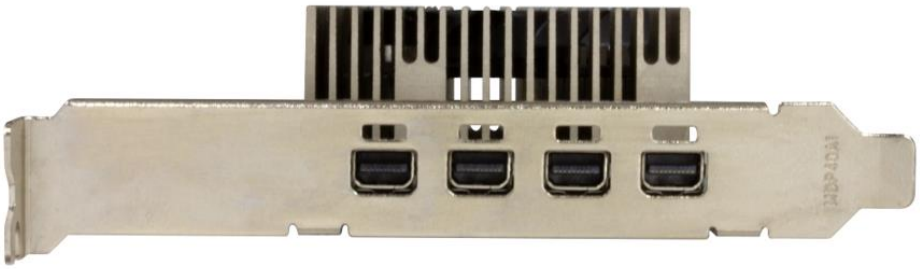
Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
24	HSOn(2)	Differential pair	GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(3)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4, Differential pair	RSVD	Reserved
34	HSOn(4)		GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	
37	HSOp(5)	Transmitter Lane 5, Differential pair	GND	Ground
38	HSOn(5)		GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSOp(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSOn(6)		GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSOp(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSOn(7)		GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground

4. Board Configuration

4.1 Board Dimension



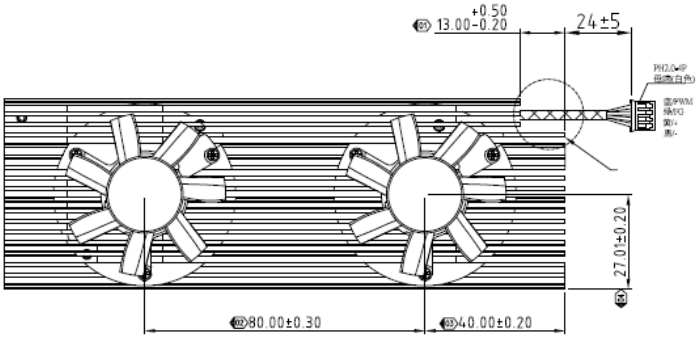
4.2 Display Interface

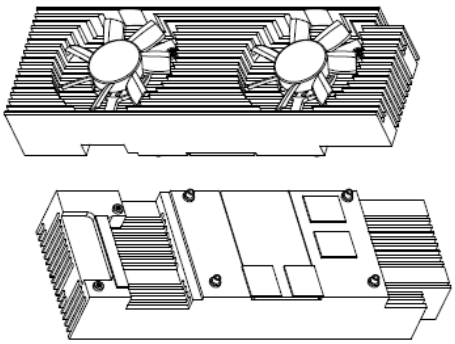


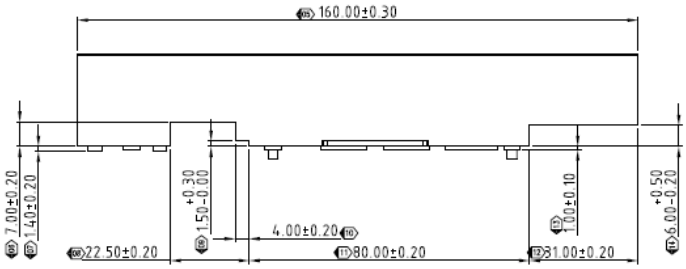
5. Thermal Mechanism

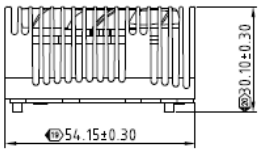
5.1 Fan Thermal Module

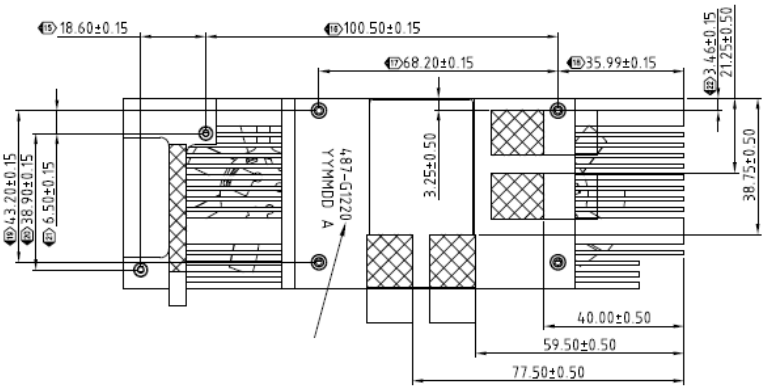
(Unit : mm)











Change log list

Rev.	Data	History
1.0	2023/08/15	EP23GL-MP4U datasheet