

## PCLD-8813

# Advanced Signal Conditioning Board for PCIe-1812/1813

## Startup Manual

### Overview

The PCLD-8813 is an advanced signal condition board designed for PCIe-1812/1813. This board features one reserved slot for every channel for plugging in a PCLD-8811 active filter board and supports isolation transfers for DI/O and counter functions.

### Features

- Isolation signal transfers for DI/O and counter
- 1 x reserved slot for every channel for plugging in a PCLD-8811 active filter board
- 2,500 V<sub>DC</sub> DI/O isolation protection
- 500 mA maximum loading per DO channel
- DIN-rail mount kit for easy mounting

### Board Components

#### Ordering Information

- PCLD-8813 advanced signal conditioning board for PCIe-1812/1813

#### Accessories

##### Wiring Cables

- PCL-101100R-1E 100-pin SCSI shielded cable, ribbon-to-pin, 1 m
- PCL-101100R-2E 100-pin SCSI shielded cable, ribbon-to-pin, 2 m

##### Signal Conditioning Boards

- PCLD-8811-AE low-pass active filter board
- PCLD-8813-AE advanced signal conditioning board for PCIe-1812/1813

For more information on this and other Advantech products, please visit our website at

<http://www.advantech.com>

For technical support and service, please visit our support website at

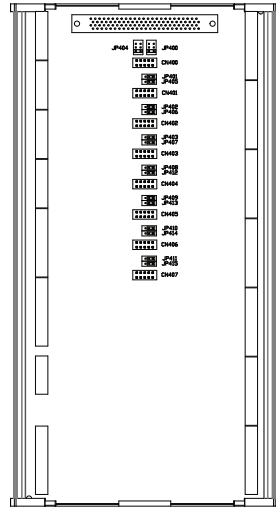
<http://support.advantech.com>

This manual is for PCLD-8813.

Part No. 2001881300

Edition 1  
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### Board Components (Cont.)



## Specifications

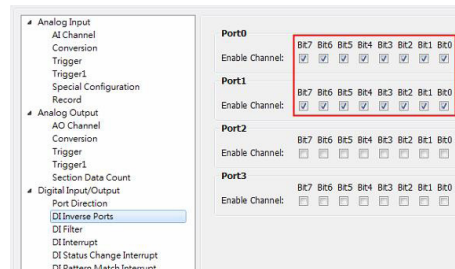
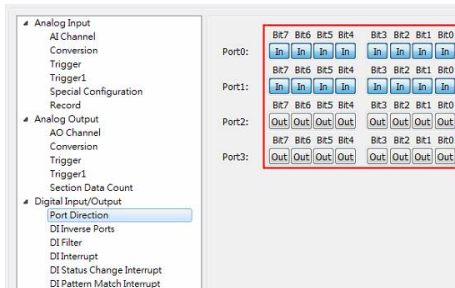
### Isolated Digital Input

Input Channels	16
Input Voltage	Logic 0: 3 V max. Logic 1: 10 V min. (30 V <sub>DC</sub> max.)
Input Current	10 V <sub>DC</sub> @ 2.97 mA
	20 V <sub>DC</sub> @ 6.35 mA
	30 V <sub>DC</sub> @ 9.37 mA
Isolation Protection	2,500 V <sub>DC</sub>
Overvoltage Protection	70 V <sub>DC</sub>
ESD Protection	2,000 V <sub>DC</sub>
Opto-Isolator Response	50 us

### Isolated Digital Output

Output Channels	16
Output Type	Sink (NPN)
Isolation Protection	2,500 V <sub>DC</sub>
Output Voltage	5 ~ 40 V <sub>DC</sub>
Sink Current	500 mA max./channel
Opto-Isolator Response	50 us

### D/I/O Configuration for PCIe-1812/1813



## Specifications (Cont.)

### Encode Counter Input

Axes	4 (independent)	
Optical Isolation	2,500 V <sub>DC</sub>	
Max. Input Pulse Frequency	10 MHz	
Input Voltage (Single Ended)	VIH (max.)	12 V
	VIH (min.)	2.8 V
	VIL (max.)	0.8 V
Input Voltage (Diff. Ended)	VIH	"CH+" – "CH-" > 0.2 V
	VIH	"CH+" – "CH-" < -0.2 V
	Max. Input Voltage	± 12 V

### CJC Calibration

$$V_t = 10 \text{ (mV/}^\circ\text{K)} \times T \text{ (}^\circ\text{K)}$$

V<sub>t</sub>: calibration voltage

T: measured temperature in °K

0 °C = 273 °K

### General Specifications

Power Supply Output	+5 V	100 mA
	+12 V	50 mA
I/O Connector Type	1 x 100-pin pin-type SCSI (for PCIe-1812/1813) 4 x 7-pin screw terminal block, 3.81 mm (for I/O) 10 x 10-pin screw terminal block, 3.81 mm (for I/O) 1 x 3-pin screw terminal block, 3.81 mm (for power output)	
Dimensions	288 x 153 x 56 mm (11.4 x 6.0 x 2.2 in)	
Power Consumption	+5 V	0.03 A typical, 0.04 A max.
	+12 V	0.15 A typical, 0.2 A max. (without PCLD-8811)
Temperature	Operating	0 ~ 60 °C (32 ~ 140 °F)
	Storage	-20 ~ 70 °C (-4 ~ 158 °F)
Relative Humidity	Operating	10 ~ 90% RH non-condensing
	Storage	5 ~ 95% RH non-condensing
Certifications	CE	

# Component Descriptions and Settings

62	ECOM1	GND_ISO		61
63	ID18	ID17		60
64	ID19	ID16		59
65	ID110	ID15		58
66	ID111	ID14		57
67	ID112	ID13		56
68	ID113	ID12		55
69	ID114	ID11		54
70	ID115	ID10		53
71	GND_ISO	ECOM0		52
72	PCOM0			
73	ID00			
74	ID01			
75	ID02			
76	ID03			
77	ID04			
78	ID05			
79	ID06			
80	ID07	+5V		51
81	GND_ISO	D6ND		50
82	PCOM1	+12V		49
83	ID08	AO_CONV		48
84	ID09	D6ND		47
85	ID10	RSV		46
86	ID11	D6ND		45
87	ID12	AI_CONV		44
88	ID13	RSV		43
89	ID14	D6ND		42
90	ID15	D6ND		41
91	GND_ISO	DTRG1		40
92	CNT0_CLK/A+	DTRG0		39
93	CNT0_CLK/A-	AGND		38
94	CNT0_B+	ATRGI		37
95	CNT0_B-	AGND		36
96	CNT0_GATE/Z+	ATRGO		35
97	CNT0_GATE/Z-	AGND		34
98	CNT0_SCLK/L+	AO1_OUT		33
99	CNT0_SCLK/L-	AO1_REF		32
100	CNT0_OUT	AGND		31
101	GND_ISO	AO0_OUT		30
102	CNT1_CLK/A+	AO0_REF		29
103	CNT1_CLK/A-	AGND		28
104	CNT1_B+	A17-		27
105	CNT1_B-	A17+		26
106	CNT1_GATE/Z+	AGND		25
107	CNT1_GATE/Z-	AGND		24
108	CNT1_SCLK/L+	A16-		23
109	CNT1_SCLK/L-	A16+		22
110	CNT1_OUT	AGND		21
111	GND_ISO	A15-		20
112	CNT2_CLK/A+	A15+		19
113	CNT2_CLK/A-	AGND		18
114	CNT2_B+	AGND		17
115	CNT2_B-	A14-		16
116	CNT2_GATE/Z+	A14+		15
117	CNT2_GATE/Z-	AGND		14
118	CNT2_SCLK/L+	A13-		13
119	CNT2_SCLK/L-	A13+		12
120	CNT2_OUT	AGND		11
121	GND_ISO	AGND		10
122	CNT3_CLK/A+	A12-		9
123	CNT3_CLK/A-	A12+		8
124	CNT3_B+	AGND		7
125	CNT3_B-	AGND		6
126	CNT3_GATE/Z+	A11-		5
127	CNT3_GATE/Z-	A11+		4
128	CNT3_SCLK/L+	AGND		3
129	CNT3_SCLK/L-	AGND		2
130	CNT3_OUT	A10-		1
131	GND_ISO	A10+		1

PCIE-1812

62	ECOM1	GND_ISO		61
63	ID18	ID17		60
64	ID19	ID16		59
65	ID110	ID15		58
66	ID111	ID14		57
67	ID112	ID13		56
68	ID113	ID12		55
69	ID114	ID11		54
70	ID115	ID10		53
71	GND_ISO	ECOM0		52
72	PCOM0			
73	ID00			
74	ID01			
75	ID02			
76	ID03			
77	ID04			
78	ID05			
79	ID06			
80	ID07	+5V		51
81	GND_ISO	D6ND		50
82	PCOM1	+12V		49
83	ID08	AO_CONV		48
84	ID09	D6ND		47
85	ID10	RSV		46
86	ID11	D6ND		45
87	ID12	AI_CONV		44
88	ID13	RSV		43
89	ID14	D6ND		42
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101	GND_ISO	AO0_OUT		30
102	CNT1_CLK/A+	AO0_REF		29
103	CNT1_CLK/A-	AGND		28
104	CNT1_B+	EX3-		27
105	CNT1_B-	EX3+		26
106	CNT1_GATE/Z+	RS3-		25
107	CNT1_GATE/Z-	RS3+		24
108	CNT1_SCLK/L+	A13-		23
109	CNT1_SCLK/L-	A13+		22
110	CNT1_OUT	QTR/SC2		21
111	GND_ISO	EX2-		20
112	CNT2_CLK/A+	EX2+		19
113	CNT2_CLK/A-	RS2-		18
114	CNT2_B+	RS2+		17
115	CNT2_B-	A12-		16
116	CNT2_GATE/Z+	A12+		15
117	CNT2_GATE/Z-	QTR/SC1		14
118	CNT2_SCLK/L+	EX1-		13
119	CNT2_SCLK/L-	EX1+		12
120	CNT2_OUT	RS1-		11
121	GND_ISO	RS1+		10
122	CNT3_CLK/A+	ATI-		9
123	CNT3_CLK/A-	ATI+		8
124	CNT3_B+	QTR/SC0		7
125	CNT3_B-	EX0-		6
126	CNT3_GATE/Z+	EX0+		5
127	CNT3_GATE/Z-	RS0-		4
128	CNT3_SCLK/L+	RS0+		3
129	CNT3_SCLK/L-	AT0-		2
130	CNT3_OUT	AT0+		1
131	GND_ISO			1

PCIE-1813

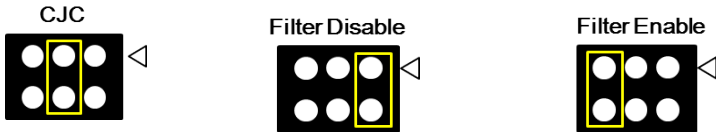
## Component Descriptions and Settings (Cont.)

### CN400 to CN407: Pin Header for PCLD-8811 Filter Board

Pin Header	Filter Board Mapping Table		
	AI Channel (single ended)	AI Channel (differential)	Jumper
CN400	AI0, AI1	AI0	JP400, JP404
CN401	AI2, AI3	AI1	JP401, JP405
CN402	AI4, AI5	AI2	JP402, JP406
CN403	AI6, AI7	AI3	JP403, JP407
CN404	AI8, AI9	AI4	JP408, JP412
CN405	AI10, AI11	AI5	JP409, JP413
CN406	AI12, AI13	AI6	JP410, JP414
CN407	AI14, AI15	AI7	JP411, JP415

### JP400 and JP404: For CJC and Jumper Settings

The PCLD-8810 provides onboard cold junction compensation (CJC) for thermocouple measurement. By setting jumpers JP400 and JP404, users can control the switching of the CJC and filter circuitry. The jumper settings are as shown below.



### JP401 to JP403 and JP405 to JP415: Filter Settings

